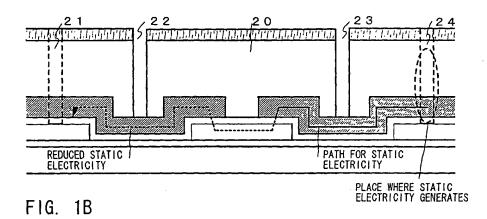
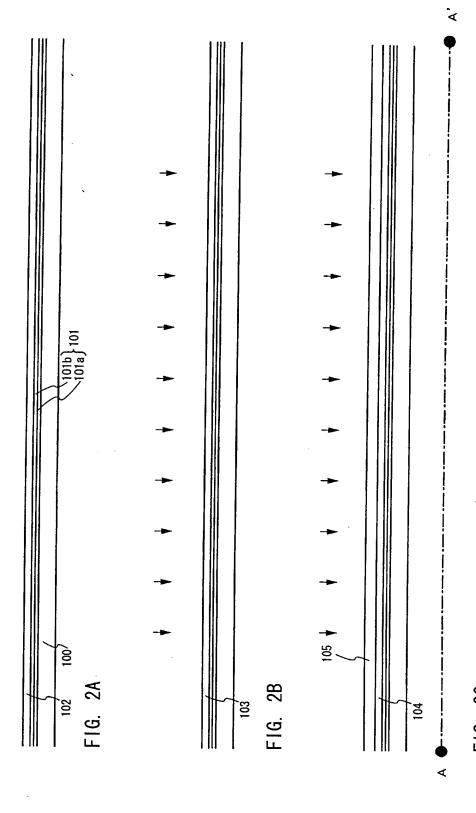


FIG. 1A

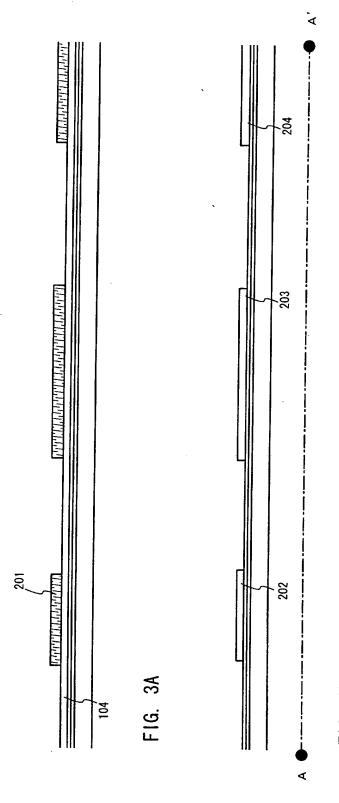


12 13 11

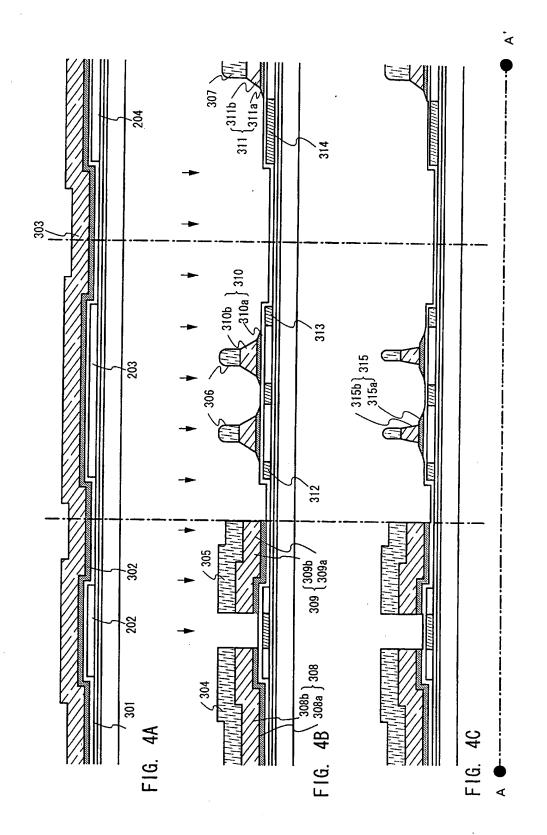
FIG. 1C



F16. 20

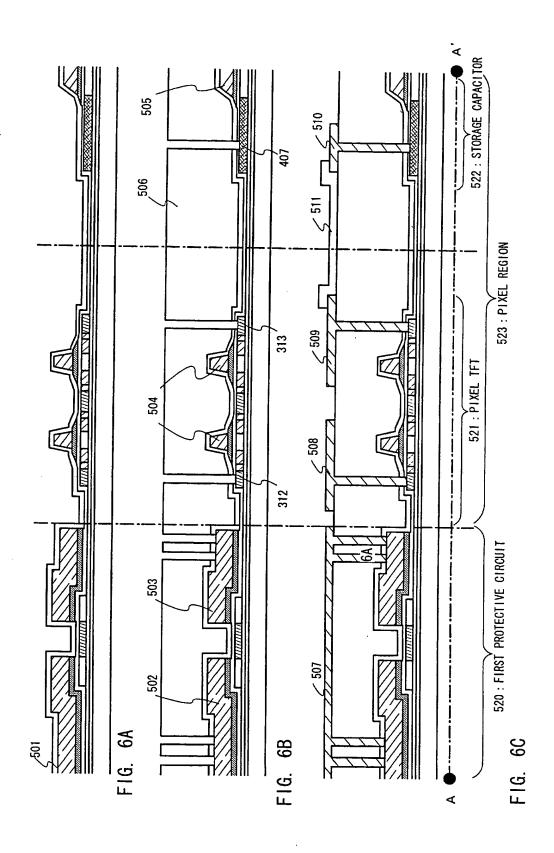


F1G. 3B



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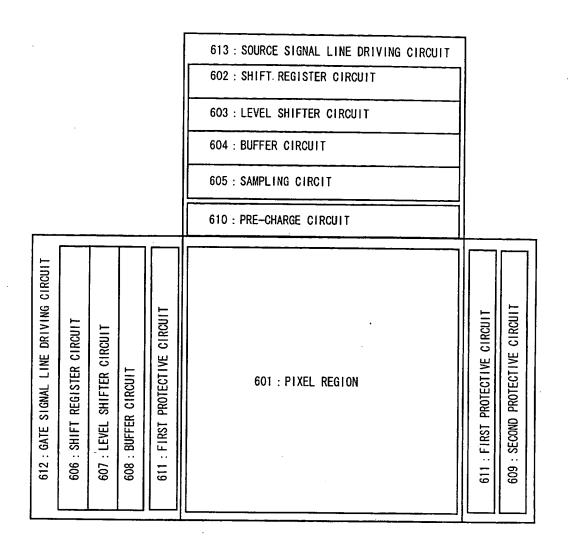


FIG. 7

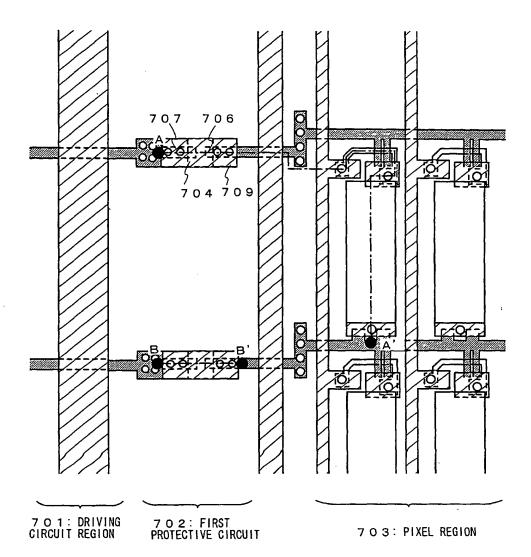


FIG. 8A

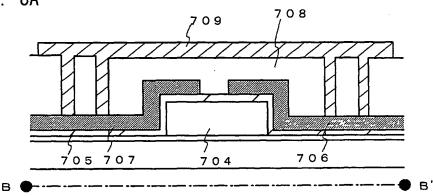


FIG. 8B

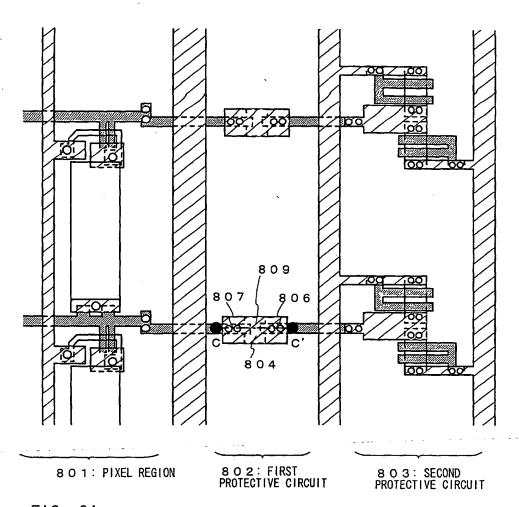
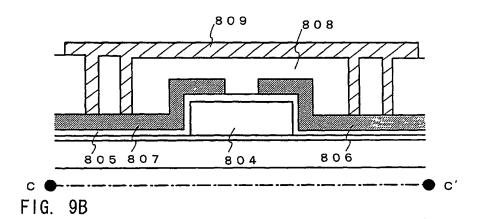


FIG. 9A



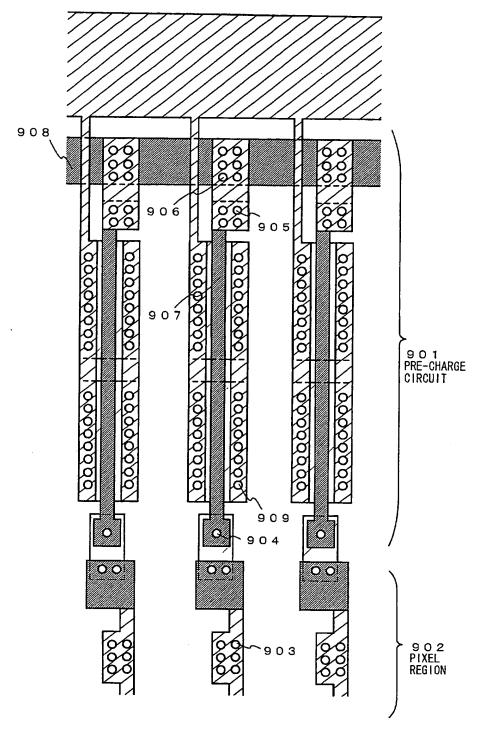


FIG. 10

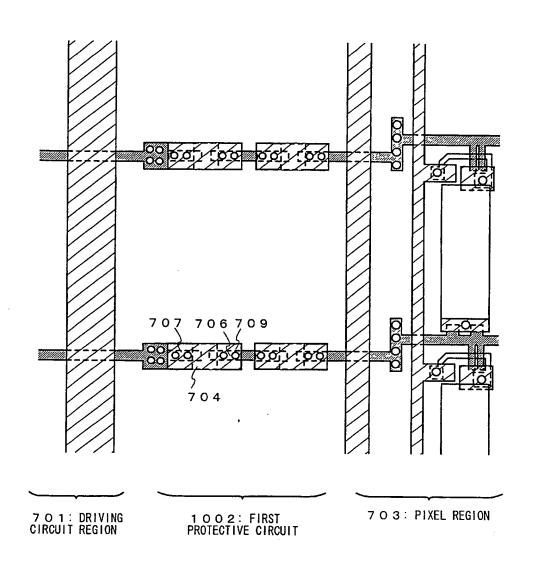


FIG. 11

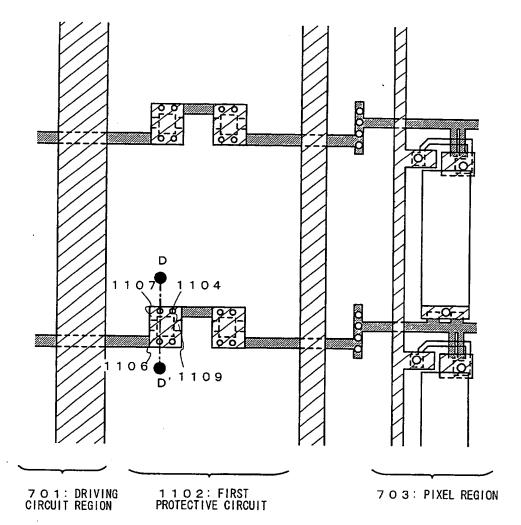
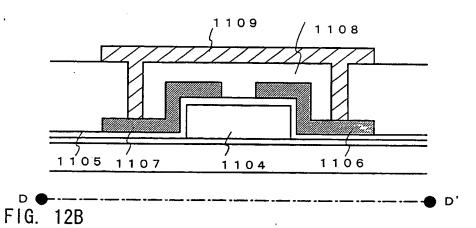
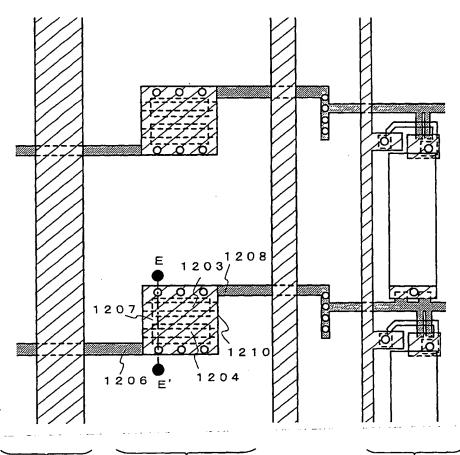


FIG. 12A



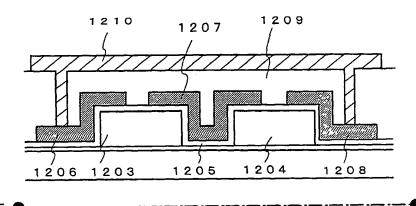
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7 O 1: DRIVING CIRCUIT 1 2 O 2: FIRST PROTECTIVE REGION CIRCUIT

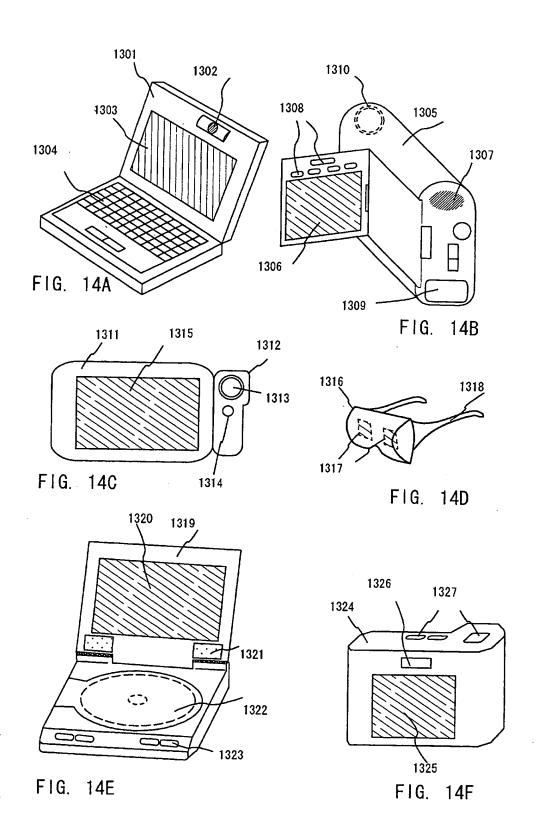
7 O 3: PIXEL REGION

FIG. 13A

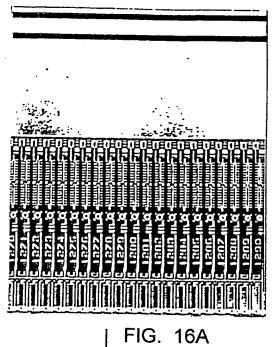


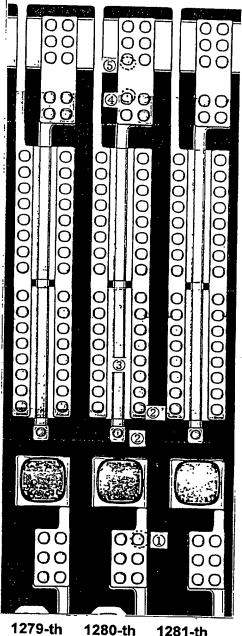
E ●-------FIG. 13B

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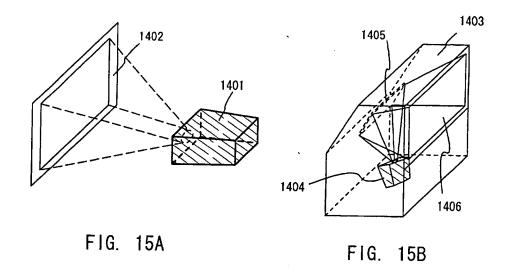
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FIG. 16B



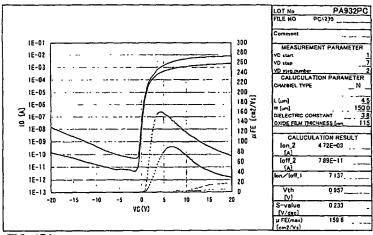


FIG. 17A

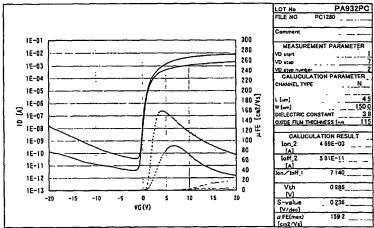


FIG. 17B

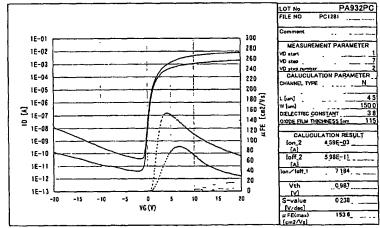


FIG. 17C

·	1712 : SOURCE SIGNAL LINE DRIVING CIRCUIT 1702 : SHIFT REGISTER CIRCUIT 1703 : LEVEL SHIFTER CIRCUIT 1704 : BUFFER CIRCUIT 1705 : SAMPLING CIRCUIT 1706 : PRE-CHARGE CIRCUIT	
1711: GATE SIGNAL LINE DRIVING CIRCUIT 1707: SHIFT REGISTER CIRCUIT 1708: LEVEL SHIFTER CIRCUIT 1709: BUFFER CIRCUIT	1701 : PIXEL REGION	1710 : PROTECTIVE CIRCUIT

FIG. 18

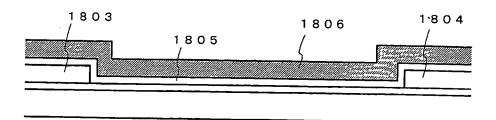
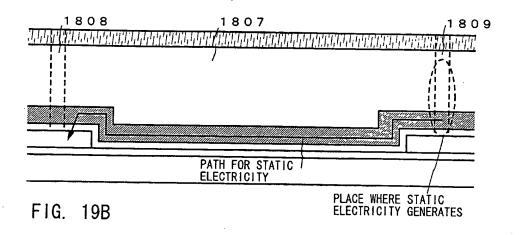


FIG. 19A



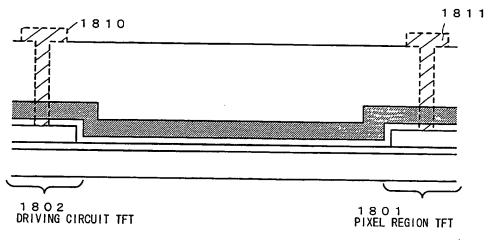


FIG. 19C

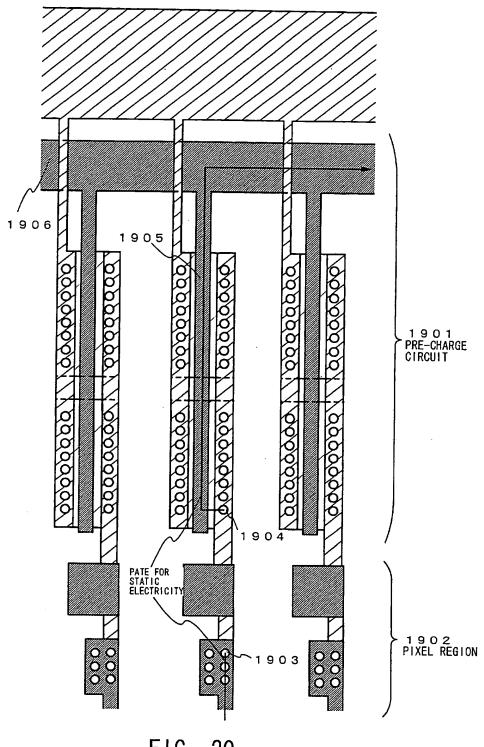


FIG. 20